ABSTRACT OF THE DISCLOSURE

An address range of consecutive instructions stored in an instruction buffer is set in an address table. A determination unit determines whether an instruction address outputted from a CPU core falls within the address range set in the address table. A selector selectively outputs an instruction code stored in the instruction buffer and an instruction code stored in an instruction cache in accordance with a determination result of the determination unit. Therefore, in the case where the CPU core fetches an instruction stored in the instruction buffer, an access cycle is guaranteed and an operation of the instruction cache is stopped, thereby making it possible to improve power efficiency.